Document # 13-52-15	**Title:** QMC6308 Preliminary Datasheet	**Rev:** B
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REVISION RECORD

Rev.	Date	Change Description
A	03/19/2019	Preliminary Version
B	04/01/2019	1) Add Register block definition 2) Change the linearity condition 3) Change top and bottom view pad name 4) Delete the RNG<1:0> definition 5) Delete the TS block definition and TS referred register output 6) Change the DRDY clear condition 7) Delete the NVM_DRY and OTP_LOAD_DONE register definition 8) Adjust the ODR setting, only keep 200Hz/100Hz 9) Change resolution value

CONTENTS

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

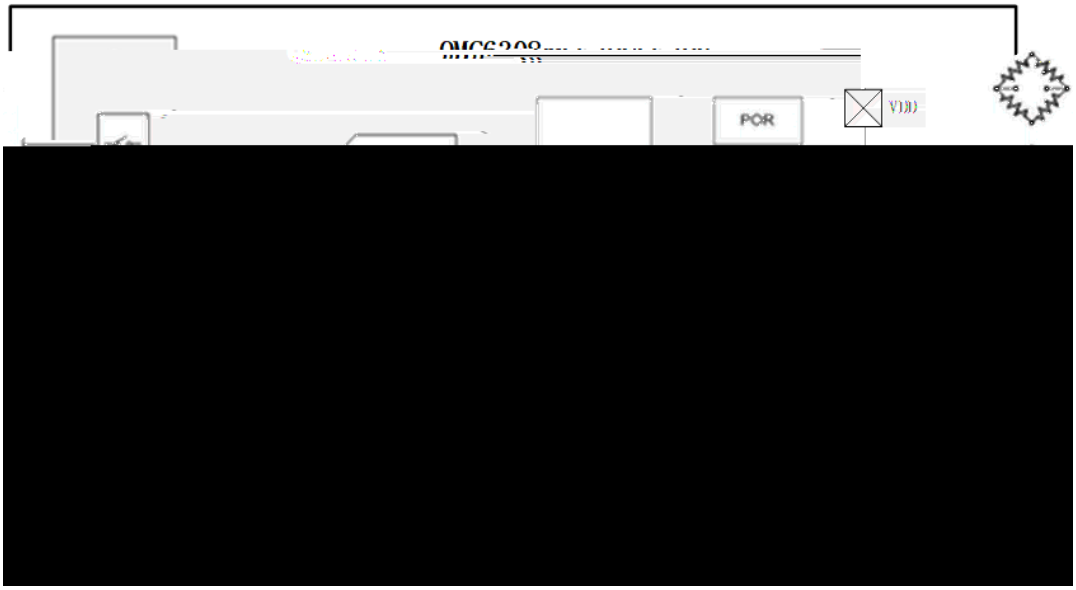


Figure 1. Block Diagram

Table 1. Block Function

Block	Function
AMR Bridge	3-axis magnetic sensor
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	Analog-to-Digital converter
Signal Conditioning	Digital blocks for magnetic signal calibration and compensations
I^2C	Interface logic data I/O
NVM	Non-volatile memory
Register	Internal register
Self-Test Driver	Internal driver to generate self-test stimulus
SET/RST Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/current reference for internal biasing
Clock Gen.	Internal oscillator for internal operation
POR	Power on reset

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (Tested and specified at 25°C except stated otherwise.)

Parameter	Conditions		Min	Typ	Max	Unit
Supply Voltage	VDD		1.65		1.95	V
Standby Current	Total Current on VDD and VLOGIC			2		F
Low power consumption	10 Measurements/second			30		uA
Max output Data Rate of Continuous Mode	OSR2 setting	OSR2=010		200		Hz
		OSR2= 011		100		Hz
Sensor Field Range	Full Scale		-30		+30	Gauss
Sensitivity [1]	Field Range = ±30G			1000		LSB/G
Linearity	Field Range = ±30G Happlied=15G			0.5		%FS
Hysteresis	All Ranges			0.3		%FS
Offset				±10		mG
Sensitivity Tempco	Ta = -40°C~85°C			±0.05		%/°C
Digital Resolution				1.0		mGauss
Field Resolution	Standard deviation OSR2=011	X/Y axis		2		mGauss
		Z axis		3		
X-Y-Z Orthogonality	Sensitivity Directions			90±1		Degree
Operating Temperature			-40		85	°C
ESD	HB Model		2000			V
	CDM		500			

Note [1]: Sensitivity is calibrated at zero field, it is slightly decreased at high fields.

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameter	MIN.	MAX.	Units
VDD	-0.3	2.0	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		50000	Gauss
Reflow Classification	MSL 1, 260 C Peak Temperature		

2.3 I/O Characteristics

Table 4. I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input High Level 1	$V_{IH}1$	SDA, SCL		1.0		1.8	V

Voltage Input Low Level 1	$V_{IL}1$	SDA, SCL		-0.3		0.45	V
Voltage Output High Level	V_{OH}	SDA	Output Current 6mA	1.2			V
Voltage Output Low Level	V_{OL}	SDA	Output Current 655zF (INT) Output Current 6r F (SDA)			0.3	V

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a positive output reading in normal measurement configuration.

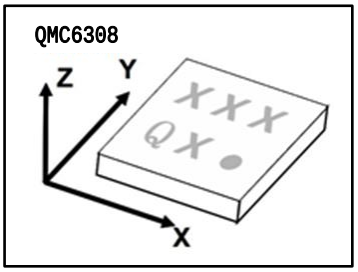


Figure 2. Package 3-D View

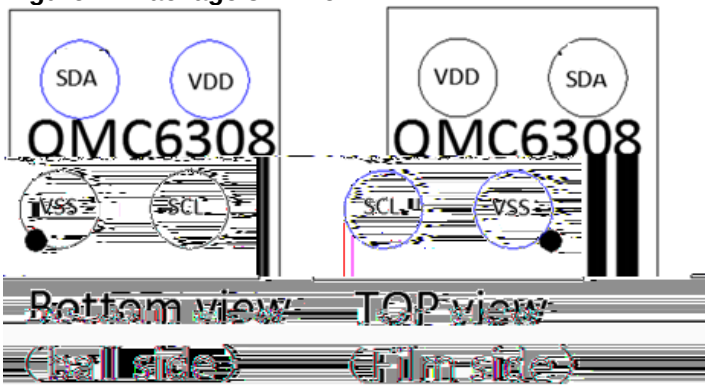


Figure 3. Package

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	TYPE	Function
A1	VSS		Power	Ground
A2	SCL	I	CMOS	I2C clock
B1	VDD		Power	Supply Voltage
B2	SDA	I/O	CMOS	I2C data

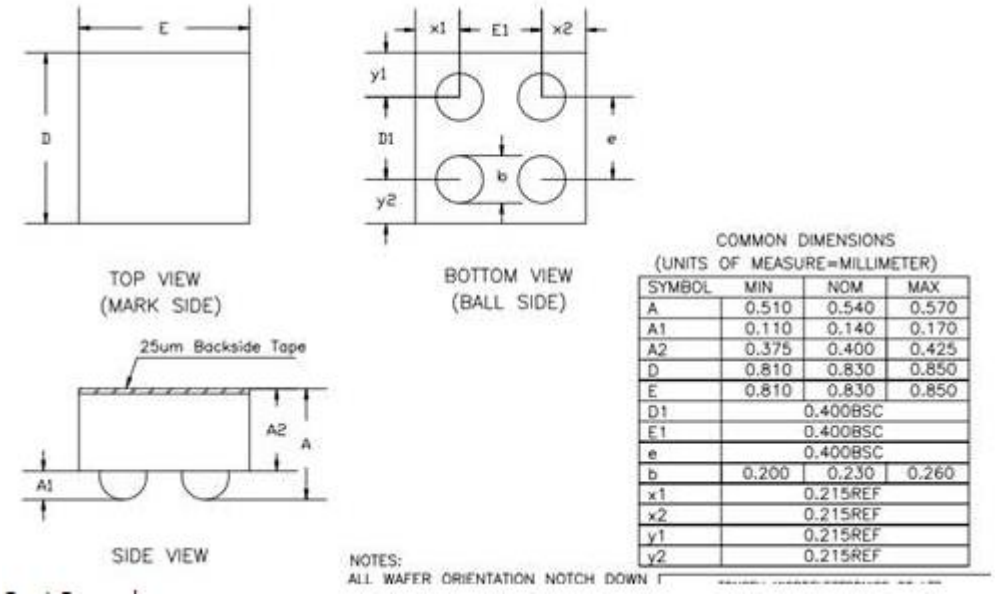
3.2 Package Outlines

3.2.1 Package Type

WLCSP

3.2.2 Package Size:

0.8mm (Length)*0.8mm (Width)*0.5mm (Height)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.510	0.540	0.570
A1	0.110	0.140	0.170
A2	0.375	0.400	0.425
D	0.810	0.830	0.850
E	0.810	0.830	0.850
D1		0.400BSC	
E1		0.400BSC	
e		0.400BSC	
b	0.200	0.230	0.260
x1		0.215REF	
x2		0.215REF	
y1		0.215REF	
y2		0.215REF	

Figure 4. Package Size

3.2.3 Marking:

Tracking code:

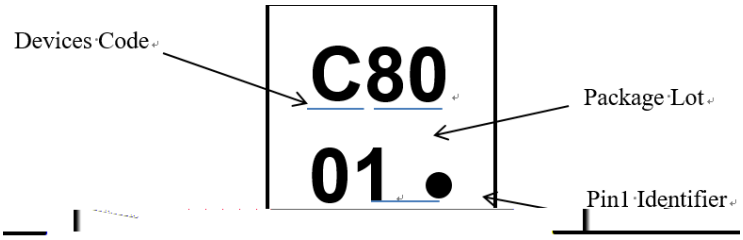


Figure 5. Chip Marking

4 EXTERNAL CONNECTION

4.1 Recommended external connection

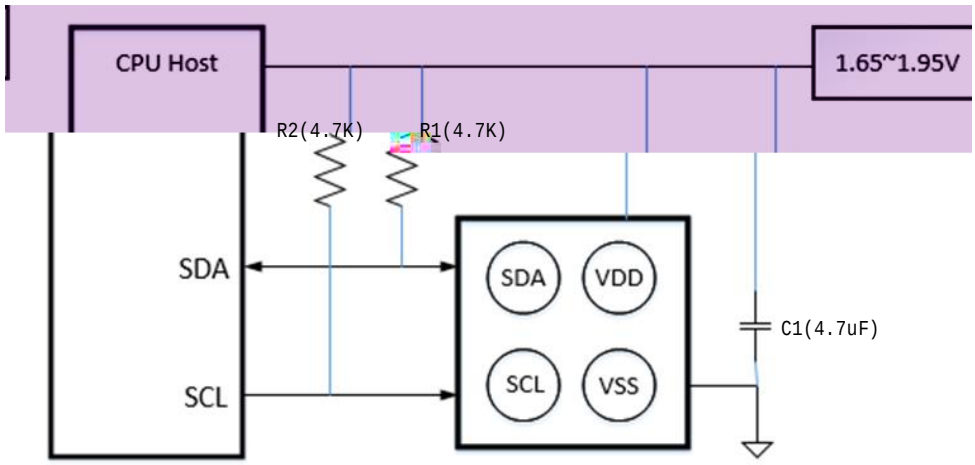


Figure 6. External Connection

4.3 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the QMC6308. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

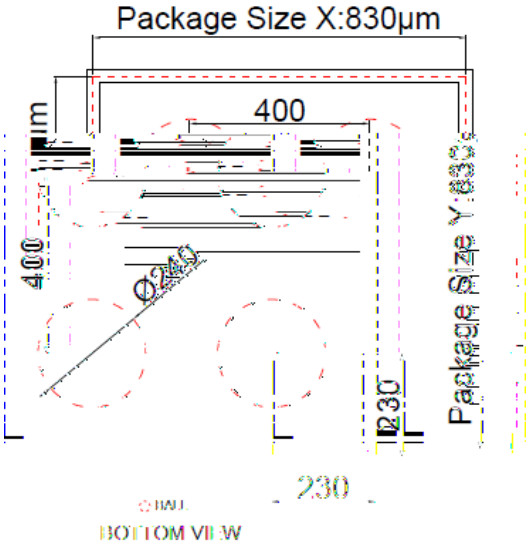


Figure 7. QMC6308 PCB footprint

4.4 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

4.4.1 Solder Paste

A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

4.4.2 Reflow Assembly

This device is classified as MSL 1 with 260 C peak reflow temperature. Reference IPC/JEDEC standard J-STD-

033 for additional information.

No special reflow profile is required for QMC6308, which is compatible with lead eutectic and lead-free solder paste reflow profiles. QST recommends adopting xt ci wfuf xy %s f szkf hyzw wx%o zmi qps x3Mf si %xt ci wsl %x%st y% recommended.

4.4.3 External Capacitors

The external capacitors C1 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 4.7 µF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors(0201) to gain low ESR characteristics.

5 BASIC DEVICE OPERATION

5.1 Anisotropic Magneto-Resistive Sensors

The QMC6308 magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the QMC6308 doess y%s i %t %f qgwfy e every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

5.2 Power Management

There are only one power supply pins to the device. VDD provides power for all the internal analog and digital functional blocks and I/O.

When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commands.

Table 6 provides references for 2 power states.

Table 6: Power States

Power State	VDD	Power State description
1	0V	Device Off, No Power Consumption
2	1.65V~1.95V	Device On, Normal Operation Mode, Enters Standby Mode after POR

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-x ht si 3%Mt w%y%xs y% controlled by the device. The Power ’ On ’ Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD at Operating Voltage to Ready for I²C Commend and Analogy Measurement.			200	uS
Power off Voltage	SDV	Voltage that Device Considers to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			uS

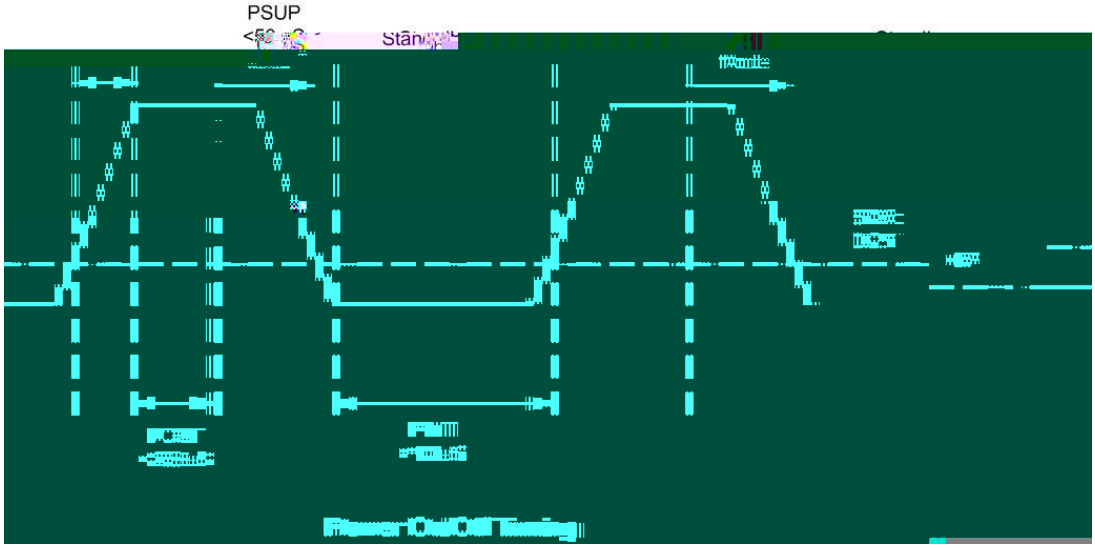


Figure 8. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C Bus Specification. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There are only one I²C address available. The default value is 2CH.

If more I²C address options are required, please contact factory.

5.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

6 MODES OF OPERATION

6.1 Modes Transition

The device has three different modes, controlled by register (0x0A), mode bits Mode<1:0>. The main purpose of these modes is for power management . The modes can be transited from one to another, as shown below, through I²C commands of changing mode bits. The default mode is Suspend Mode.

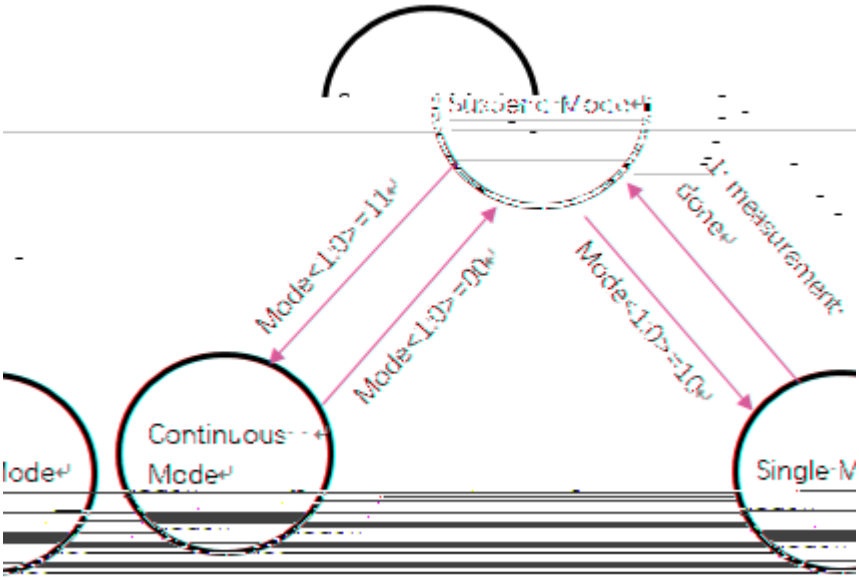


Figure 9. Modes Transition

6.2 Description of Modes

6.2.1 Continuous Mode

During the Continuous mode (MODE bits

7 Application Examples

7.1 Continuous Mode Setup Example

- ✧ Write Register 0BH by 0x00 (Define Set/Reset mode, with Set/Reset On)
- ✧ Write Register 0AH by 0x63 (Define OSR2=011, set continuous mode)

7.2 Measurement Example

- ✧ Check status register 09H[0] , 1 means ready.
- ✧ Read data register 01H ~ 06H.

7.3 Suspend Mode Example

- ✧ Write Register 0AH by 0x00

7.4 Soft Reset Example

- ✧ Write Register 0BH by 0x80

8 I²C COMMUNICATION PROTOCOL

8.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 8. I²C Timings

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock		f_{scl}		0		400	kHz
SCL Low Period		t_{low}		1			X
SCL High Period		t_{high}		1			X
SDA Setup Time		t_{sudat}		0.1			X
SDA Hold Time		t_{hddat}		0		0.9	X
Start Hold Time		t_{hdsta}		0.6			X
Start Setup Time		t_{susta}		0.6			X
Stop Setup Time		t_{susto}		0.6			X
New Transmission Time		t_{buf}		1.3			X
Rise Time		t_r					X
Fall Time		t_f					S

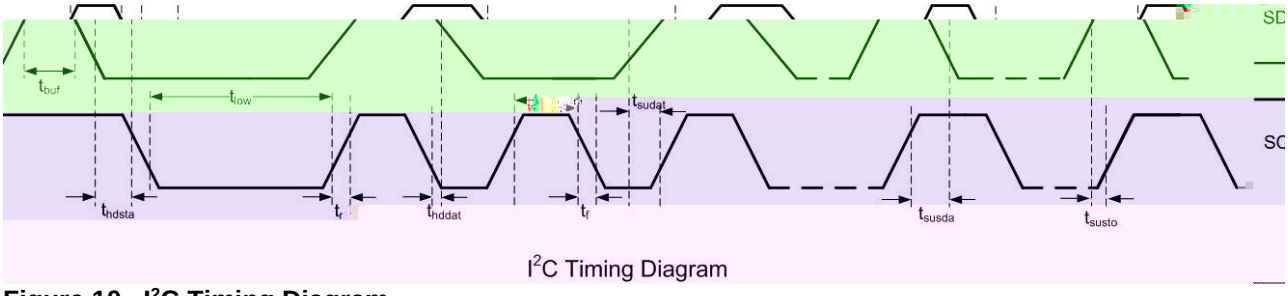


Figure 10. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 9. Abbreviation

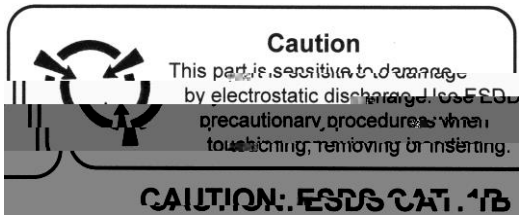
SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: [illegible] down the SDA

ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
QMC6308-TR	-40°C ~ 85°C	WLCSP	Tape and Reel: 5k pieces/reel



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China Patents 201210563667.3, 201210563956.3, 201210563952.5, 201210563687.0, 201310403912.9, 201410027189.3, 201410027240.0, 201410027085.2 and 201410085278.3 apply to the technology described.